

501.18758C13



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: K. SHIMOHIGASHI et al.
Serial No.: Not Yet Assigned
Filed: September 14, 1994
For: SEMICONDUCTOR MEMORY
Group: 2511
Examiner: T. Fears

PRELIMINARY AMENDMENT

Honorable Commissioner of
Patents and Trademarks
Washington, D.C. 20231

September 15, 1994

Sir:

Prior to examination, please amend the above-identified
application as follows:

IN THE CLAIMS

Please cancel claims 1-19 without prejudice or
disclaimer.

Please add the following new claims:

-- 26.¹ A semiconductor memory comprising:
a pair of data lines which are formed substantially
in parallel to each other;
a plurality of word lines, each of which is arranged
so as to intersect with both of said data lines of said pair
of data lines;

A2
Contd

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